

2 GHz 1V Sub-mW, Fully Integrated PLL for Clock Recovery Applications Using Self-Skewing

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Abstract—This paper describes the design of a fully integrated phase-locked loop for clock and data recovery applications. A two-stage ring oscillator modified for high-speed applications is proposed. The new proposed two-stage VCO features a self-skewing local action per stage. This leads to a significant improvement in speed up to 3 times than the conventional one. An operation up to 2GHz under 0.9mW power consumption with 1V supply is achieved using a standard 0.18 μm process. The chip active area is 0.1x0.1 mm².

Keywords: low voltage, low power, two-stage ring VCO, self-skewing.

I. INTRODUCTION

HIGH-SPEED low power clock recovery circuits find wide applications in high performance communication systems [1]. Clock and data recovery (CDR) is a key block in the receiver that extracts the clock signal and removes unwanted jitter. The clock extraction allows synchronous operations. The design of the CDR presents special challenges especially when the supply voltage is reduced.

The trend in the use of low-voltage power supplies for CMOS integrated circuits is set by the reliability issue of small size MOSFET transistors and the increasing use of low-weight long life battery-operated portable electronic systems. Portable equipment has been required to operate with a single-battery supply voltage. Hence, considering today's technical trends, the importance and necessity of circuit engineering for very low-voltage operation are continually increasing.

A key and critical building block in both wireless and optical communications transceivers is the voltage-controlled oscillator (VCO). Due to the reduction of the power consumption of digital circuits and the scaling of modern technologies, the supply voltages of integrated circuits continue to decrease towards sub-1V.

A CMOS VCO can be built using ring structures, relaxation circuits, or an LC resonant circuit. The LC design has the best noise and frequency performance owing to the large quality factor Q achievable with resonant networks [2]. However, adding high-quality inductors increases the cost and complexity of the chip in a CMOS process flow, and also introduces problems such as the control of eddy currents. Ring oscillators, on the other hand, can be built in any standard CMOS process and require less die area than LC designs. In addition the ring architectures can be used to provide multiple output phases and wide tuning ranges. The concept of skewed-delay [3] can also be used to improve the performance for the multi-stage ring VCO.

This paper describes the design of a low power 2GHz, 1V PLL circuit. The design was implemented in a standard 0.18 μm process. A modified two-stage ring VCO that improves the overall characteristics of conventional ring oscillators is also introduced. The new proposed two-stage VCO features a self-skewing local action per stage. This achieves higher frequency and wider tuning range.

Section II describes the system architecture. The PLL circuit implementation of each building block is presented in section III. The PLL layout is outlined in section IV. In section V, The overall system simulation results are reported and compared to previously published work. Finally, conclusions are drawn in section VI.

II. ARCHITECTURE

The phase locked loop is a basic building block in data recovery systems. The PLL is used for clock recovery, and then the data can be retrieved using a decision circuit. A random data type has some properties that directly influence the design of clock and data recovery circuits. The choice of the CDR architecture is primarily determined by the speed and supplies voltage limitations of the technology as well as the power dissipation and jitter requirements of the system. A simplified block diagram of the CDR architecture is illustrated in Fig. 1.

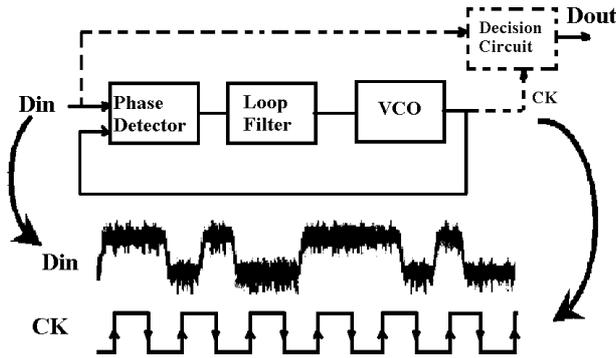


Figure 1. Block diagram of a generic CDR architecture.

The CDR architecture generally consists of four building blocks (Fig. 1):

- 1) phase detector, detecting the phase difference between the data and the recovered clock
- 2) loop filter
- 3) voltage controlled oscillator (VCO)
- 4) decision circuit, retiming the data and reducing its jitter.

III. PLL CIRCUIT IMPLEMENTATION

The PLL architecture is fully differential to suppress the common-mode noise and provide robust operation under low voltage operation, using a typical 1V supply.

A. XOR Phase Detector

A high-speed XOR gate is used as a phase detector suitable for RZ data-format. It locks onto a signal with 90 degrees phase offset if the VCO center frequency is precisely equal to the data rate. The schematic of a fully differential XOR gate is shown in Fig.2. To obtain high frequency performance; the MOS Current Mode Logic (MCML) is adopted to maximize the speed and improve the common-mode performance [4].

B. Loop Filter

The output of the XOR signal is filtered using a simple first order passive RC network. The low pass filter averages the signal and yields the required DC level that controls the VCO. This design adopted a 20K Ω loop resistor and a capacitor of 0.7pF. Under these conditions, a filter cutoff frequency of one-hundredth the input frequency is obtained, which can easily be integrated on-chip.

C. Self-Biasing Cell

In order to improve the jitter performance, a low-noise biasing cell is used for more linear Voltage-Frequency characteristics, as shown in Fig.3. Moreover, the biasing generator circuit is used to increase the tuning range and linearity of the VCO [5]. Thus, the VCO control voltage can operate from 0V to VDD.

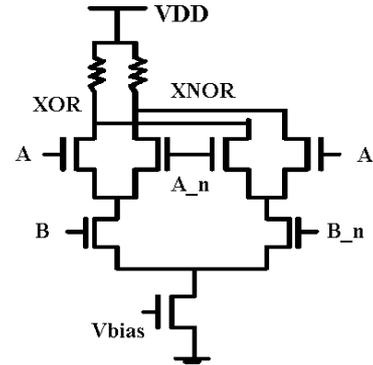


Figure 2. MCML XOR Gate.

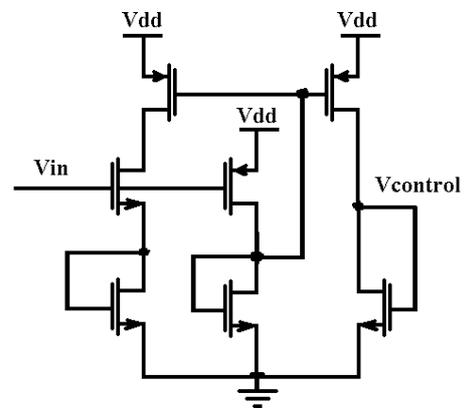


Figure 3. Self biasing cell.

D. VCO Design

The VCO ring architecture is used to provide multiple output phases and wide tuning ranges. The VCO topology proposed in this paper considerably reduces the supply voltage requirement, and consequently the power consumption. The concept of the negative skewed-delay cell is illustrated in Fig.4 [3], which is extended and modified in this paper. It consists of a conventional CMOS inverter and a conceptual negative delay element inserted at one of the two transistor inputs of the CMOS inverter. In this case, the input of the PMOS is connected to the negative delay elements and the input signal to the PMOS comes earlier than that of the NMOS. In conventional inverter delay cells, the input signals are simultaneously provided from the previous stage.

In contrast, the new proposed two stages VCO features a self-skewing local action per stage. This leads to a significant improvement in speed up to 3 times faster than the conventional one. The VCO can be easily implemented with a multi-stage ring oscillator. In the two-stage based VCO, only two phases are present so there are no skewed phases. The presented two-stage ring VCO uses a local delayed version of the same input designed to be a skewed phase of the same clock using simple delay blocks.

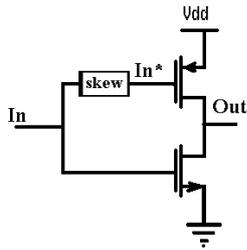


Figure 4. Schematic diagram for the skewed delay cell [3].

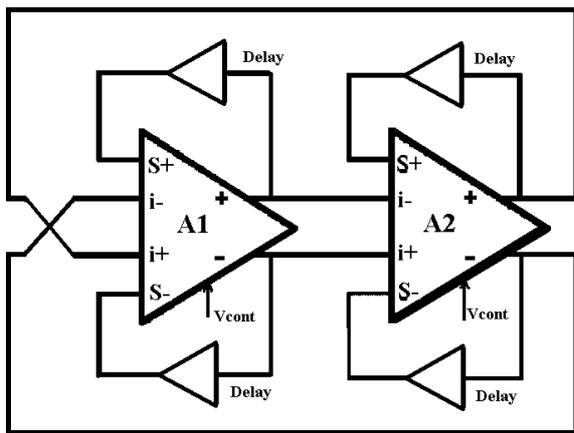


Figure 5. Block diagram of the modified two-stage ring VCO proposed in this work.

A two stage-ring VCO was chosen to be used in the PLL circuit for its low power consumption, and low noise. The conventional two-stage ring VCO is commonly implemented using two negative gm delay cells. Each delay cell is based on the regenerative cross-coupled PMOS transistors. This allows for rail-to-rail output signals and full switching of the FETs in the stage. A maximum frequency of 750MHz has been attained under 1V operation.

Adopting phase skewing, the VCO delay stage can increase the maximum frequency of oscillation in the case of three or more stages as reported in [6] under 1.8V supply voltage. This is done if the skewed phases at one stage are extracted from a different stage [5], [6].

The proposed two-stage ring oscillator presented is modified for higher oscillation frequency. The new proposed two-stage VCO features a self-skewing local action per stage. To get a local skewed phase of the clock, two delay blocks were added per stage to provide the required skewing as shown in Fig.5.

The schematic of the unit delay cell is shown in Fig.6. The transistors M1 and M2 are the differential input pair. The devices M3 and M4 are the negative gm cross-coupled pair. M5 and M6 provide the skewing action through the two delay blocks. Each delay block is a double CMOS inverter as shown. These inverters provide a skewed version of the input.

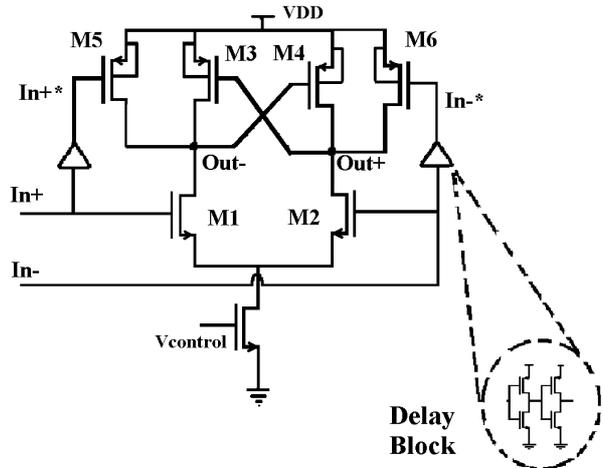


Figure 6. Schematic of the proposed self-skewing delay cell used in two-stage ring VCO.

The simulation results show that the phase noise of the proposed two-stage ring VCO is -90dBc/Hz at a 1MHz offset from a 2GHz center frequency. A summary of the VCO performance of both conventional and modified is listed in Table1.

The new proposed VCO features a 3X higher maximum operating frequency. A 10X enhancement in the tuning range is also achieved. This improvement in speed and tuning range is achieved at the cost of an expected 40% increase in power consumption. However, the entire design is still low-power thanks to the 1V supply.

TABLE I. PERFORMANCE OF THE TWO-STAGE VCOS.

Topology	f_o (GHz) Max	Tuning range %	Power mW
2-stage (Conventional)	0.7	8%	0.45 @ 0.7GHz
2-stage (Modified)	2.2	80%	0.70 @ 2.0GHz
Adv./Disadv.	+	+	-

IV. LAYOUT

The circuit layout was executed using the Virtuoso layout tool in the Cadence Design Environment. The active area required for implementation of the proposed PLL is only $0.1 \times 0.1 \text{ mm}^2$, where no special mask is required for the layout. The layout, shown in Fig.7, was implemented in a standard $0.18\mu\text{m}$ process.

The on-chip loop filter resides in the upper left, where a poly resistance has been used to implement the loop resistor and the capacitor has been realized as a MOS-transistor gate. A comparable area is required for the XOR phase detector, which is located at the lower left. The ring oscillator is located in the top right area where matching between transistor pairs have been considered. Both the biasing cell and the VCO output buffer can be seen in the lower right corner.

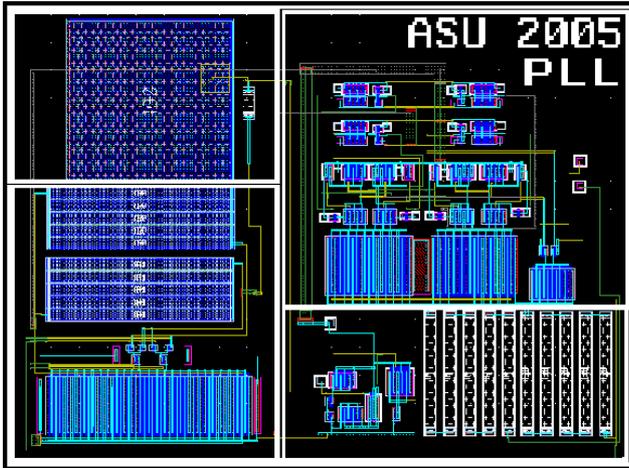


Figure 7. PLL circuit layout.

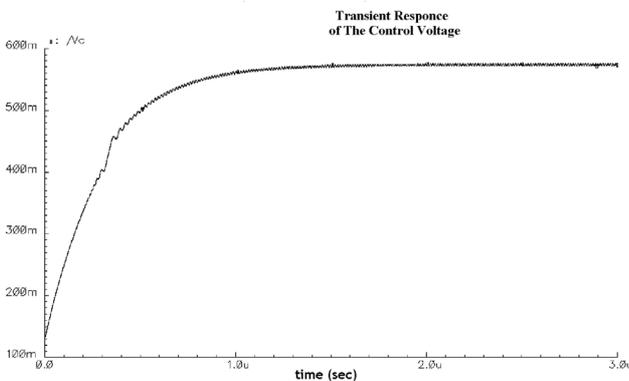


Figure 8. The control voltage versus time.

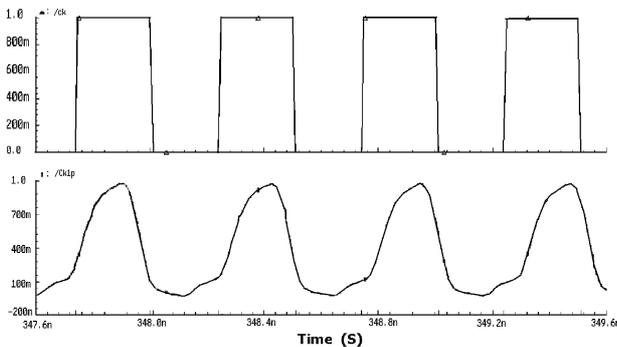


Figure 9. The input and output clocks under lock condition.

V. PLL SIMULATION RESULTS

All simulation results presented have been obtained using SpectreRF simulations. The control voltage, shown in Fig.8, reaches lock condition within a pull-in time of 0.8 μ s. The input and output clocks are shown Fig.9. The VCO output signals running at 2GHz have full swing. The simulation was carried out with an input frequency of 2GHz.

Compared to that published in [5], the simulation results showed a higher operating frequency of wider tuning range and lower power consumption of the same supply voltage. The performance comparison to the work published in [5], using the same process and working from a similar supply, is displayed in Table 2. This work offers higher speed operation under lower power consumption with faster settling time.

TABLE II. COMPARISON WITH RECENTLY PUBLISHED 1V-PLL WITH RING VCO

	This work	[5]
Process	0.18 μ m	0.18 μ m
Supply Voltage	1V	1V
Operating frequency range	0.6– 2.2 GHz	50 – 1100MHz
Locking time	0.8 μ s	3.6 μ s
Power Consumption	0.9mW@2GHz	1.1mW@1GHz
Chip area	0.1x0.1 mm ²	NA

VI. CONCLUSION

The design of a 2GHz fully integrated phase-locked loop for clock and data recovery applications with a 1V supply voltage has been presented. A high-speed low-voltage ring-based VCO modified for higher operating frequency has been proposed, implemented and simulated. The new proposed two stages VCO features a self-skewing local action per stage. This leads to a significant improvement in speed up to 3 times than the conventional one. An operation up to 2.2GHz was reported. Also the use of self-biasing cell increases the tuning range and the tuning linearity of the VCO. A power consumption of 0.9mW at 2GHz is achieved under 1V supply using a standard 0.18 μ m process with a chip active area of 0.1x0.1 mm².

VII. REFERENCES

- [1] M. Soyuer, "A monolithic 2.3-Gb/s 100mW clock and data recovery circuit in silicon bipolar technology," IEEE J. Solid-State Circuits, vol.28, pp. 1310-1313, Dec. 1993.
- [2] J. Savoj, and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector", IEEE J. Solid-State Circuits, vol. 36, no. 5, pp. 761-768, may 2001.
- [3] S. Lee, B. Kim, and K. Lee, "A Novel High-Speed Ring Oscillator for Multiphase Clock Generation Using Negative Skewed Delay Scheme," IEEE J. Solid-State Circuits, Vol. 32 No2, pp. 289-291, Feb 1997.
- [4] H. Bui, and Y. Savaria, "10 GHz PLL Using Active Shunted-Peaked MCML Gates and Improved Frequency Acquisition XOR Phase Detector in 0.18 μ m CMOS," IEEE International Workshop on System-on-Chip (IWSOC), 2004.
- [5] K. Cheng, C. Lai and Yu-Lung Lo, "A CMOS VCO for 1V, 1GHz PLL Applications," IEEE, IEEE Asia-Pacific Conference on Advanced System Integrated Circuits (AP-ASIC), Aug 2004.
- [6] Y. Eken, and J. P. Uyemura, "A 5.9-GHz Voltage-Controlled Ring Oscillator in 0.18 μ m CMOS," IEEE Journal of Solid-State Circuits, Vol. 39, No.1, pp. 0230-233, Jan 2004.